CLAIMS

What is claimed is:

1. A method for treating a deposited high-k gate dielectric layer during fabrication of a semiconductor device, the method comprising:

nitriding a deposited high-k gate dielectric layer prior to forming a gate electrode;

performing a first anneal of the deposited high-k dielectric in a non-oxidizing ambient prior to forming a gate electrode; and

performing a second anneal of the deposited high-k dielectric in an oxidizing ambient prior to forming a gate electrode.

2. The method of claim 1, wherein the second anneal is performed after nitriding the high-k dielectric layer and after performing the first anneal.

3. The method of claim 2, wherein the first anneal is performed prior to nitriding the high-k dielectric layer.

4. The method of claim 3, wherein the first anneal is performed at a temperature of about 1000 degrees C or less.

5. The method of claim 4, wherein the first anneal is performed at a temperature of about 900 degrees C or less.

6. The method of claim 5, wherein the first anneal is performed at a temperature of about 700 degrees C or more.

7. The method of claim 5, wherein the non-oxidizing ambient of the first anneal comprises N_2, Ar, He, or Ne.

8. The method of claim 4, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

9. The method of claim 3, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

10. The method of claim 3, wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in a nitrogen containing ambient.

11. The method of claim 10, wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3.

12. The method of claim 3, wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process.

13. The method of claim 3, wherein the second anneal is performed at a temperature of about 1000 degrees C or less.

14. The method of claim 2, wherein the first anneal is performed after nitriding the high-k dielectric layer.

15. The method of claim 14, wherein the first anneal is performed at a temperature above about 1000 degrees C.

16. The method of claim 15, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

17. The method of claim 14, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

18. The method of claim 14, wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in a nitrogen containing ambient.

19. The method of claim 18, wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3.

20. The method of claim 14, wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process.

21. The method of claim 14, wherein the second anneal is performed at a temperature of about 1000 degrees C or less.

22. The method of claim 2, wherein the second anneal is performed at a temperature of about 1000 degrees C or less.

23. The method of claim 22, wherein the second anneal is performed at a temperature of about 700 degrees C or less.

24. The method of claim 23, wherein the second anneal is performed at a pressure of about 1 Torr or less.

25. The method of claim 23, wherein the second anneal is performed at atmospheric pressure.

26. The method of claim 22, wherein performing the second anneal comprises exposing the high-k dielectric layer to an oxidizing liquid solution.

27. The method of claim 26, wherein the oxidizing liquid solution comprises $H_2O + H_2O_2$.

28. The method of claim 26, wherein the oxidizing liquid solution comprises $H_2O + O_3$.

29. The method of claim 26, wherein the oxidizing liquid solution is taken from the group consisting of $H_2SO_4 + H_2O_2 + H_2O$, $H_2SO_4 + H_2O$, $HNO_3 + H_2O$, $HNO_3 + H_2O_2 + H_2O$, $HCl + H_2O_2 + H_2O$, and $NH_4OH + H_2O_2 + H_2O$.

30. The method of claim 22, wherein the second anneal is an oxidizing plasma process.

31. The method of claim 22, wherein the second anneal is an ozone anneal.

32. The method of claim 22, wherein the second anneal is a low temperature anneal with UV excitation in an oxidizing ambient.

33. The method of claim 1, wherein the first and second anneals are performed prior to nitriding the high-k dielectric layer.

34. The method of claim 33, wherein the first anneal is performed at a temperature of about 1000 degrees C or less.

35. The method of claim 34, wherein the first anneal is performed at a temperature of about 900 degrees C or less.

36. The method of claim 35, wherein the first anneal is performed at a temperature of about 700 degrees C or more.

37. The method of claim 35, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

38. The method of claim 34, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

39. The method of claim 33, wherein the non-oxidizing ambient of the first anneal comprises N2, Ar, He, or Ne.

40. The method of claim 33, wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in a nitrogen containing ambient.

41. The method of claim 40, wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3.

42. The method of claim 33, wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process.

43. The method of claim 33, wherein the second anneal is performed at a temperature of about 1000 degrees C or less.

44. The method of claim 33, further comprising performing a third anneal in a non-oxidizing ambient after nitriding the deposited high-k dielectric layer.

45. The method of claim 44, wherein the third anneal is performed at a temperature above about 1000 degrees C.

46. The method of claim 45, wherein the non-oxidizing ambient of the third anneal comprises N2, Ar, He, or Ne.

47. The method of claim 44, wherein the non-oxidizing ambient of the third anneal comprises N2, Ar, He, or Ne.

48. The method of claim 44, wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in a nitrogen containing ambient.

49. The method of claim 48, wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3.

50. The method of claim 44, wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process.

51. The method of claim 44, wherein the first anneal is performed prior to performing the second anneal.

52. The method of claim 44, further comprising performing a fourth anneal in an oxidizing ambient after performing the third anneal.

53. The method of claim 52, wherein the fourth anneal is performed at a temperature of about 700 degrees C or less.

54. The method of claim 53, wherein the fourth anneal is performed at a pressure of about 1 Torr or less.

55. The method of claim 53, wherein the fourth anneal is performed at atmospheric pressure.

56. The method of claim 52, wherein performing the fourth anneal comprises exposing the high-k dielectric layer to an oxidizing liquid solution.

57. The method of claim 56, wherein the oxidizing liquid solution comprises $H_2O + H_2O_2$.

58. The method of claim 56, wherein the oxidizing liquid solution comprises $H_2O + O_3$.

59. The method of claim 56, wherein the oxidizing liquid solution is selected from the group consisting of $H_2SO_4 + H_2O_2 + H_2O$, $H_2SO_4 + H_2O$, $HNO_3 + H_2O$, $HNO_3 + H_2O_2 + H_2O$, $HCl + H_2O_2 + H_2O$, and $NH_4OH + H_2O_2 + H_2O$.

60. The method of claim 52, wherein the fourth anneal is an oxidizing plasma process.

61. The method of claim 52, wherein the fourth anneal is an ozone anneal.

62. The method of claim 52, wherein the fourth anneal is a low temperature anneal with UV excitation in an oxidizing ambient.

63. The method of claim 1, wherein nitriding the deposited high-k gate dielectric layer comprises performing a nitridation anneal in a nitrogen containing ambient.

64. The method of claim 63, wherein the nitridation anneal is performed at a temperature of about 1000 degrees C or less and wherein the nitrogen containing ambient comprises NH_3.

65. The method of claim 1, wherein nitriding the deposited high-k gate dielectric layer comprises performing a plasma nitridation process.

66. A method of fabricating a transistor gate structure, the method comprising:

depositing a high-k gate dielectric layer above a semiconductor body;

nitriding a deposited high-k gate dielectric layer;

performing a first anneal of the deposited high-k gate dielectric in a non-oxidizing ambient;

performing a second anneal of the deposited high-k gate dielectric in an oxidizing ambient;

forming a gate electrode material layer above the gate dielectric layer after nitriding and after performing the first and second anneals; and

patterning the gate electrode and gate dielectric layers to form a patterned gate structure.

67. A method of treating a high-k gate dielectric layer, the method comprising:

performing one or more pre-nitridation anneal processes of a deposited high-k gate dielectric prior to forming a gate electrode;

performing a nitridation process after the pre-nitridation anneal processes; and

performing one or more post-nitridation anneal processes of a deposited high-k gate dielectric after the nitridation process and prior to forming a gate electrode.